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Electrode metallization for high permittivity oxide RF thin film capacitors

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Abstract

High permittivity oxide thin film capacitors for RF components should be integrated on the chip to form a complete miniaturized module, with other semiconductor or thin film components such as inductors, isolation capacitors, and bias resistors. The quality factor (Q) values of the RF capacitors are strongly dependent on electrode conductivity. Alas the best conducting metals (e.g. Ag, Cu, Al) are not thermodynamically stable during deposition of high permittivity oxide films with high temperature and oxygen atmosphere. On the other hand, refractory metals (e.g. Mo, W) endure high temperatures, but are prone to oxidation. Therefore, a diffusion barrier is a prerequisite for integrating refractory metals to achieve a stable electrode structure.

In this study both non-reactive and sacrificial diffusion barriers with Mo metallization were investigated on Si/SiO_2 substrates. Also, noble metals (Au and Pt) as oxidation resistant materials were examined. Annealing at 650 °C was performed to the electrode stacks in an open-end air furnace and in vacuum with protective gas.

The chemically inert materials Au and Pt failed to endure the high annealing temperature. Au became extremely rough and cracks appeared. Massive grain growth and adhesion loss occurred with Pt film. Mo electrode withstood the oxidizing ambient conditions with a sacrificial Si or Al–Ti diffusion barrier. Moderate increase in surface roughness was observed after the annealing due to oxidation. Also, thermally stable AlN, Si_3N_4, and SiO_2 diffusion barriers were able to block oxygen from the Mo electrode.

Keywords: Films; Surfaces; Diffusion; Capacitors; Electrode

1. Introduction

Electrodes, especially the bottom electrode, have an important role in the performance of a high permittivity thin film capacitor structure. The surface of the electrode for a capacitor structure should be as smooth as possible. Any texture on the surface creates leakage current and problems with further processing of the device. The stack must be thermally stable, i.e. no reactions must take place between substrate and thin films at elevated temperatures. In RF applications Q value of the component usually depends primarily on the resistance of the electrodes. High resistivity adds series resistance in a capacitive component, lowering the Q value. High permittivity insulating layers are usually deposited at elevated temperatures (≥650 °C). Moreover, to restore oxygen stoichiometry, the deposition process is regularly carried out using oxygen atmosphere. In addition, matching the coefficient of thermal expansion (CTE) of substrate, bottom electrode layer, and the growing dielectric is required.

Such conditions pose severe challenges to the development of the capacitor structure. Potential materials that have low resistivity include Ag, Al, Au, Cu, and some refractory metals. All the well-conducting face-centered cubic (fcc) metals melt in rather low temperatures. This makes them quite unstable surfaces for dielectric deposition. On the other hand, high melting point refractory metals, e.g. W and Mo are thermally stable materials at elevated temperatures. Also their resistivity is suitable for RF integration. The disadvantage with Mo and W is their affinity to oxygen.

The main two possibilities for the integration of the bottom electrodes are: the noble metals (Au, Ag, platinum metals) and the refractory metals (Mo, W, Ta, and Nb) with a protective barrier. The diffusion barrier can either be a sacrificial layer or thermally stable insulator/compound layer. In addition, matching the coefficient of thermal expansion of substrate, bottom electrode layer, and the growing dielectric is required.

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Pt and Pd are too resistive to be used alone in RF applications. Oxidation resistance of Au and Pt makes them potential alternatives in the use of electrode material. According to the literature, noble metals have been applied in capacitive structures.[1] The drawback with the use of Pt is that its oxygen permeability is high, which causes problems to the substrate.[2–5] When taking the high processing temperature into account, Ag and Al must be excluded. Cu and Au are borderline cases, however, Cu metallization with an Al–Ti oxygen diffusion barrier have been reported.[6] The use of W for electrode metallization can be found in literature.[7] Additionally, conducting oxides like RuO_2 and IrO_2 have been investigated, but mostly for memory applications.[8]

This paper will focus on stable electrode metallization structures for RF high permittivity thin film devices.

2. Materials and methods

The examined electrode film stacks were deposited onto n-type (100)-oriented thermally oxidized silicon wafers by dc magnetron sputtering. The investigated diffusion barriers were either sputtered reactively or processed in plasma enhanced chemical vapor deposition (PECVD) reactor.

Deposition rate, intrinsic stresses, and thicknesses of the processed films were measured by Veeco Dektak 200 Si profilometer. The resistance of the processed films was analyzed by four-point probe measurements (Loresta AP). Surface morphology was analyzed by using a Digital Instruments Dimension 3001 atomic force microscope (AFM) in tapping mode. A cross-sectional analysis was conducted with a LEO 1560 scanning electron microscope (SEM).

Electrode stacks were annealed severely in an open-end air furnace at 650 °C for 30 min. Also vacuum furnace with protective Ar gas was used in this study.

3. Results and discussion

The RF losses of the capacitive thin film devices are expressed in terms of an equivalent circuit of a resistor in series with a capacitor. The quality factor Q is the ratio of reactance to the series loss resistance. The device Q_{tot} consist of losses caused by the dielectric Q_{die} and the conductor Q_{ele}. The total Q value of the capacitor is:

$$Q_{tot} = \frac{Q_{die} Q_{ele}}{Q_{die} + Q_{ele}} \quad (1)$$

As the frequency is increased the effects of Q_{ele} will generally become dominant. The effect to the total Q value, caused by the electrodes, can be calculated by:

$$Q_{ele} = \frac{d_{die} d_{ele}}{\omega \varepsilon A N \rho} \quad (2)$$

where d_{die} is the thickness of the dielectric, d_{ele} electrode thickness, ω the $2\pi f$, ε relative dielectric constant, A electrode plate area, N number of squares in the electrodes, and ρ is the resistivity of the electrode material.

Table 1
Influence of electrode metal on the calculated Q value with 5.3 pF capacitance at 1 GHz frequency

	Metal			
	Au	Cu	Mo	Pt
Q_{ele}	128	179	58	28

To estimate how the electrode effects on the Q value, a typical 30 μm × 30 μm capacitor structure and a RF probe with a pitch of 150 μm is chosen as an example ($N = 5$ squares). With capacitance of 5.3 pF (insulator thickness 300 nm with ε of 200) at 1 GHz frequency and using bulk resistivities with 500 nm metal thickness the Q values of the electrodes are listed in Table 1.

As a chemically inert material Pt is an attractive electrode metal for high dielectric deposition. However, Pt itself, as a thin film, is too resistive for RF applications. To study the behavior of platinum, a thick Pt electrode film was sputtered onto Si/SiO_2 substrate with a thin TiW (5 nm) adhesion layer. After annealing in air furnace, gigantic grain growth was observed visually in 750 nm thick Pt film. Grain growth roughens the electrode surface. Also the resistivity decreased: the as-deposited film had resistivity of 17.3 μΩ cm while after annealing it was 13.5 μΩ cm. The effect is due to annealing of crystal defects in the deposited film and grain growth.

Grain growth is induced by intrinsic film stress. High stresses in sputtered films produce also hillock formation.[3,4] Stresses appeared to be inherently compressive (≥200 MPa) with the sputtering equipment employed. The adhesion layer beneath Pt also enhances the grain growth, even if it was thin,[3,4] via its migration into Pt and oxidation.[2–5] Pt has high permeability to oxygen[2–5] thus oxidation of the adhesion layer is fast. Additionally, no cracks on the surface were observed, since CTE mismatch is moderate, Pt 9.0 ppm/°C compared to the Si substrate, 2.49 ppm/°C.

While processing a thick Pt is difficult in device integration, a thin Pt electrode needs an additional parallel conductor layer to enhance RF performance. Au is a possible choice.[1] Noble metals, e.g. Au, Pt, and conditionally Ag, endure oxygen in the deposition ambient, but material recrystallization is fast at elevated temperatures. Additionally, Pt and Au form a solid solution at these process temperatures.[9]

A 500 nm Au film was annealed in vacuum furnace for 1 h at 650 °C. A large scale surface morphology change can be observed with AFM, Fig. 1. Also cracks were observed in both $Au/SiO_2/Si$ and $Au\text{-}Pt/SiO_2/Si$ structures.

During annealing the RMS roughness of the Au surface increased from 5.1 to 12.5 nm. Concurrently vertical range change was 37.7–147.1 nm. The grain coarsening and growth can be explained by recovery and recrystallization (secondary grain growth) of the processed Au film. Recrystallization and CTE mismatch with the Si substrate and Au film (14.1 ppm/°C) creates cracks and pores on the electrode film, influencing the growth of the dielectric too. Due to high CTE mismatch and recrystallization of Au, the film shrinks more than the other parts

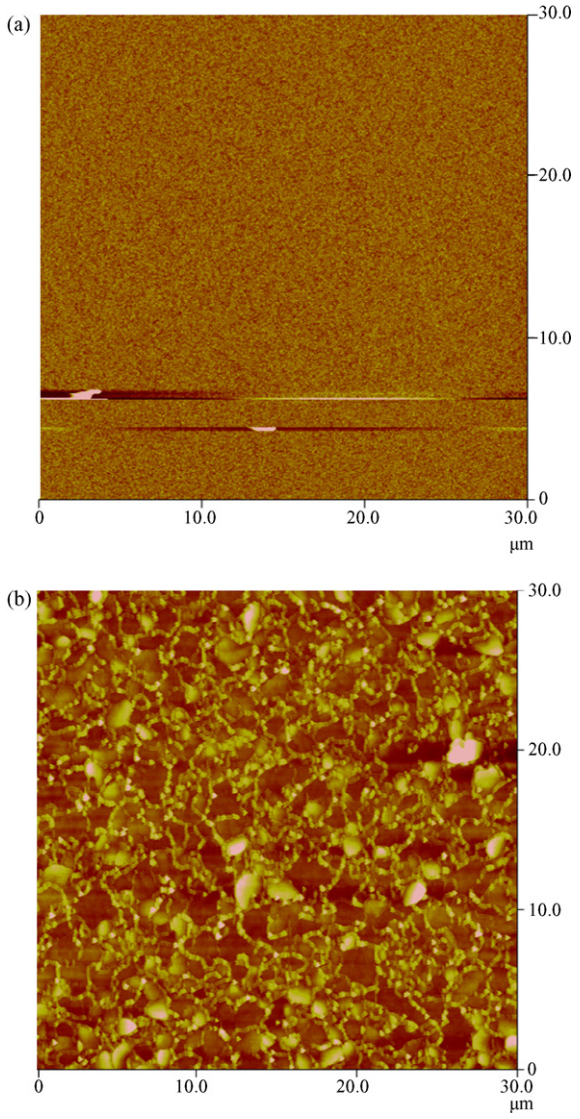

Fig. 1. AFM picture of sputtered 500 nm Au film (a) as-deposited and (b) annealed in vacuum furnace for 1 h at 650 °C. Data scale 100 nm.

of the stack causing cracks to appear during cooling sequence after annealing. Cracks create major processing problems to the following process steps.

An alternative electrode configuration is to use a refractory metal with a thin diffusion barrier against oxidation. Although refractory metals like Mo, W, Ta, and Nb are stable at elevated temperatures, they oxidize easily. At high temperatures the metals mentioned above are not self-passivating and oxygen migrates through their native oxide. For RF integration Mo and W are the most recommended choices in terms of conductivity. Although W has been integrated to capacitive structures,[7] preliminary studies using sputter deposition showed unacceptable roughness.

CTE of Mo (5.0 ppm/°C) is close to that of the substrate, indicating favorable compatibility. Mo films (470 nm) with sacrificial Si barrier layers of 40 and 80 nm were examined. These samples were annealed in air furnace for 30 min at 650 °C.

The surface of the annealed 40 nm Si sample became extremely rough. Oxidation of Si at the surface occurred and silicide formation at the interface of Mo and Si intensified the roughness. Molybdenum silicide forms at quite low temperatures, ≤400 °C.[10] Decorative oxidation of Mo columnar grains may have also taken place.

The Mo layer was intact, when the Si layer was made thicker, which means that Si works as a sacrificial diffusion barrier. With the 80 nm Si barrier, the Mo layer was not oxidized and surface of the sample was smooth. During annealing the RMS roughness of the surface changed only from 2.3 to 3.2 nm. Concurrently a vertical range shift was from 17.1 to 23.2 nm. Mo electrodes remained conductive after annealing with both barrier thicknesses. During measurement the probes were forced through the surface silicon dioxide to make contact.

Another sacrificial diffusion barrier (Al–Ti) was also studied with refractory electrode. The Al–Ti layer (75 nm in thickness) was co-sputtered from two separate pure elemental targets in ratio of 1:1, which caused the deposited film to grow in nanocrystalline or amorphous form.[11] The samples were annealed in an air furnace for 30 min at 650 °C. The Al–Ti layer reacted with the oxygen in the processing ambient leaving Mo layer underneath intact (Fig. 2).

AFM investigation was performed to analyze the electrode surface. During annealing RMS roughness of the surface

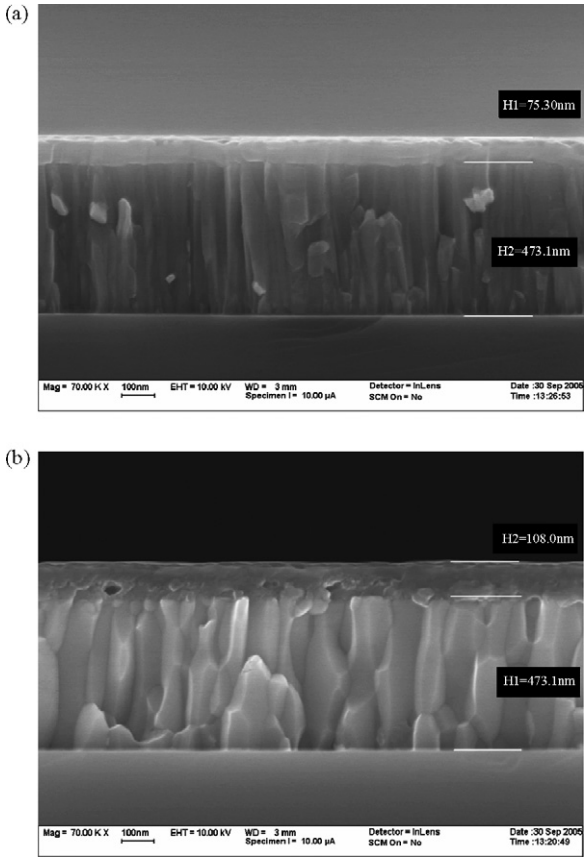

Fig. 2. SEM picture of sacrificial (Al–Ti) diffusion barrier on Mo (a) as-deposited and (b) annealed in air furnace for 30 min at 650 °C.

increased from 2.8 to 5.8 nm. Concurrently a vertical range change was from 19.8 to 49.0 nm. Mo electrode remained conductive also with Al–Ti barrier. Both stacks equipped with sacrificial barrier showed reasonable stability for integration in capacitor applications.

Another approach is to use a passive oxidation-resistant protective layer on top of the Mo conductor. Stable AlN, Si_3N_4, and SiO_2 diffusion barriers, 75 nm in thickness, were deposited onto Mo (450 nm) film. A thin Pt (75 nm) film with a TiW (2 nm) adhesion layer formed the topmost film. The samples were annealed in an air furnace same way as the sacrificial barrier samples.

Massive blistering and roughening was observed in annealing in air. Cross-sectional SEM analysis was performed to examine the integrity of the passive oxygen diffusion barriers. In Fig. 3 cross-sectional picture of the Si_3N_4 barrier, as an example, is illustrated.

All the barriers were undamaged and they protected the Mo layer underneath, indicating a good stability of the barrier against oxidation. In resistivity measurements, the topmost Pt carried the current in dc measurements and the metal resistivity in the Si_3N_4 sample decreased from 20.8 to 17.3 μΩ cm during annealing. The culprit for surface roughening was the topmost Pt layer with its adhesion layer. Pt adhesion loss and roughening were due to grain growth and hillock formation (Fig. 3) in Pt and the oxidation of the thin adhesion layer.[3,4] Cracks were not observed due to minor CTE mismatch. CTE of SiO_2 and Si_3N_4 is 0.56 and 2.44 ppm/°C, respectively.

If a Pt top layer is required, it must be deposited without adhesion layer. This can be accomplished by in situ bombardment of the substrate with Ar ions prior to the Pt deposition.

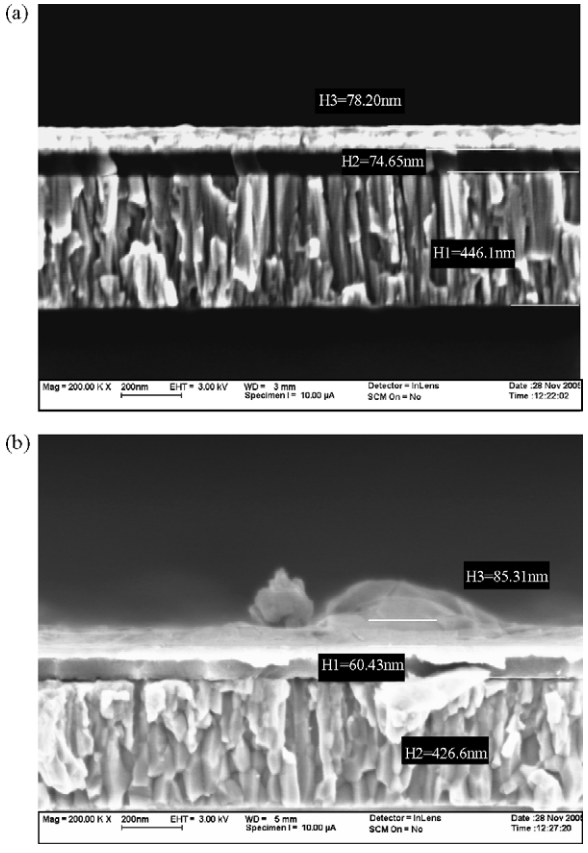

Fig. 3. SEM picture of thermally stable Si_3N_4 diffusion barrier on Mo with Pt film on top (a) as-deposited and (b) annealed in air furnace for 30 min at 650 °C.

4. Conclusions

Different metallic oxidation resistant electrode materials were tested against oxidation. A simple metallic electrode seems to be out of question to integrate in a high permittivity capacitor structure since the chemically inert materials Au and Au-Pt failed to endure the high annealing temperature (≥650 °C). Thick Pt electrode suffered from grain growth and film roughening.

Electrodes equipped with a diffusion barrier against oxidation were also examined. Mo electrode endured the oxidizing ambient conditions with a thin sacrificial Si or Al–Ti diffusion barrier. Moderate surface roughness increase as a consequence of oxidation and crystallization was observed during the annealing.

Thermally stable AlN, Si_3N_4 and SiO_2 diffusion barriers can be used for blocking the oxygen from the deposition conditions. However, electrode stack with the stable insulating barrier and a thin Pt layer failed due to oxidation of the adhesion layer of Pt. But thin platinum can be used, at least, for seed layer purposes with Ar bombarding of the electrode in situ before Pt sputter deposition. Resistivity decreased during annealing in open-end air furnace tests. The deposited Mo electrode with sacrificial and thermally stable diffusion barrier endured annealing in air at 650 °C.

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