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Short communication

Memory characteristics of multi-stacked thin films using La_2O_3 and $LaAlO_3$ as charge trap layer

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Abstract

$Al_2O_3/La_2O_3/Al_2O_3$ (ALA) and $Al_2O_3/LaAlO_3/Al_2O_3$ (A/LAO/A) multi-stacked films were deposited on Si substrates by MOCVD. No interfacial layers ($Al_xSi_yO_z$) were observed in TEM images, and the thickness ratio of the tunnel oxide (bottom oxide), trap layer (middle oxide), and blocking oxide (top oxide) was about (1:1.3:3) in both films. Memory windows of the (ALA) and (A/LAO/A) films were 1.31 V and 3.13 V, respectively. Each value in the program/erase cycle test was maintained for up to 10^4 cycles.

Keywords: Flash; ONO; Charge trap; High-*k* dielectrics; La_2O_3; $LaAlO_3$

1. Introduction

Recently, the scaling issues associated with floating-gate NAND-type flash memory devices were addressed in the 2007 ITRS roadmap, which concluded that the scale-down limit of these devices is expected to be the 30 nm technology node [1]. The continuous use of a floating-gate for charge storage has some drawbacks including a threshold voltage (V_{th}) shift and a wide distribution of V_{th}. Moreover, stress-induced leakage current (SILC) causes problems in scaling down NAND flash memory [2].

Hence, the concept of a SONOS or MONOS (silicon/metal-oxide-nitride-oxide-silicon) type memory device was proposed in order to solve these problems [3–5]. Since the SONOS (or MONOS) type device has a stacked structure, the floating gate is not necessary. Hence, the SILC is basically prevented and structural problems such as capacitance coupling can be solved [6]. However, this structure is also faced with a scale-down limitation in terms of thickness reduction [7]. In particular, the tunnel oxide (bottom oxide) problem is quite serious. As the thickness of the tunneling oxide decreases, program/erase time becomes shorter while the program/erase voltage is also reduced; however, retention in the device is thereby deteriorated. One potential way of dealing with this problem is to change the material associated with the tunnel oxide from SiO_2 to a high-dielectric (high-*k*) material [8,9]. Many research groups have already begun to investigate the possibility of using high-*k* materials instead of the ONO (oxide-nitride-oxide) structure.

In this paper, we investigate the memory characteristics of two-types of structures utilizing high-*k* materials instead of the ONO structure. We fabricated $Al_2O_3/La_2O_3/Al_2O_3$ (ALA) and $Al_2O_3/LaAlO_3/Al_2O_3$ (A/LAO/A) structures. We also analyzed memory characteristics and program/erase voltages and times of the multi-stacked films.

2. Experimental procedures

The (ALA) and (A/LAO/A) films were deposited on (1 0 0) n-type Si wafers (SILTRON, Korea) using a MOCVD system. $La(tmhd)_3$ tetraglyme adduct [Tris(2,2,6,6-tetramethyl-3,5-heptanedionato) lanthanum (III) tetraglyme adduct, $La(C_{11}H_{19}O_2)_3{\cdot}CH_3(OCH_2CH_2)_4OCH_3$, Strem chemicals Inc., USA] and Al-acetylacetonate [$Al(CH_3COCH)_3$, Strem Chemicals] were used as precursors for the La and Al metals, respectively. N_2 was used as a carrier gas. Prior to deposition, the wafers were cleaned with organic solvents. They were then treated with a 10% hydrofluoric (HF) solution to remove native oxides.

The substrate temperature was maintained at 350 °C during deposition, and the working pressure was maintained at 5 Torr

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(266.6 Pa). The (ALA) and (A/LAO/A) films were deposited by combination of Al, La precursors and O_2 gas. After Al_2O_3 (bottom oxide) layer was deposited, we had purging time for 2 min under N_2 ambience to remove Al precursor and form trap layer. Then, the La_2O_3 and $LaAlO_3$ (trap layer) layers were deposited on the Al_2O_3 (bottom oxide) layer, respectively. The purging process also progressed in same condition after trap layer deposition. Finally, Al_2O_3 (top oxide) layer was deposited on the each trap layer. All film deposition processes were performed by only changing the precursor gases in same chamber. The film thickness was measured by ellipsometry (Gaertner, L117, $\lambda = 632.8$ nm) and TEM (JEM-2100, Jeol). To measure electrical properties of the (ALA) and (A/LAO/A) films (metal – blocking oxide – trap layer – tunnel oxide – semiconductor), capacitors (Pt/Al_2O_3/La_2O_3/Al_2O_3/Si and Pt/Al_2O_3/$LaAlO_3$/Al_2O_3/Si) were fabricated. The Pt electrode of the capacitor was deposited using magnetron sputtering with shadow masks. The capacitor area was 9.25×10^{-4} cm^2 for all of the specimens. A *C–V* analysis was performed using a Keithley 590 *C–V* analyzer at 1 MHz in order to investigate memory window and the optimized program voltage.

3. Results and discussion

Fig. 1 shows TEM images of the (a) (ALA) and (b) (A/LAO/A) films. All phases in the films were amorphous. The interface of (ALA) films was rougher than that of (A/LAO/A) films, and the total thicknesses of both films were about 33.34 nm. Thicknesses of the tunnel oxide, trap layer, and blocking oxide were 6.67 nm, 8.33 nm, and 18.34 nm in the (ALA) films, respectively. On the other hand, thicknesses of tunnel oxide, trap layer, and blocking oxide were 5.56 nm, 7.22 nm, and 20.56 nm, respectively, in the (A/LAO/A) films. In general, the conduction band offset of the trap layer material should be lower than that of tunnel and blocking oxide materials. According to the conduction band offset calculated by the LDA method and experimental values for gate oxide by Maria [10] and Edge et al. [11], the offsets of Al_2O_3, La_2O_3, and $LaAlO_3$ on Si were found to be 2.8 eV, 2.3 eV, and 2.1 eV. Hence, the difference in conduction band offset for the (A/LAO/A) and (ALA) films is about 0.7 eV and 0.5 eV, respectively. Since an interfacial layer ($Al_xSi_yO_z$) was not observed in either film, we ignored structural and electrical effects of interfacial layer.

Fig. 2 shows threshold voltage (V_{th}) distributions of the (a) program mode and (b) erase mode in the (ALA) films, and (c) program mode and (d) erase mode in the (A/LAO/A) films. Trends toward the upper right in the program mode, Fig. 2(a) and (c), indicate that charge trapping phenomenon occurs primarily in the films. On the other hand, trends toward the upper right in the erase mode, Fig. 2(b) and (d), indicate that charge ejection phenomenon occurs more primarily in the silicon substrate. Prior to the program/erase operation, a full erase operation was performed at −15 V for 2 s to remove the initial charge carrier in the (ALA) and (A/LAO/A) films. Maximum program conditions (V_{th}(program) − V_{th}(full erase)) of the (ALA) and (A/LAO/A) films were 13 V for 1000 ms and 13 V 100 ms. However, these values are too high for commercial use. Hence, we concluded optimum program and erase conditions are 11 V for 10 ms for the program mode and −13 V for 100 ms for the erase mode. For (A/LAO/A) films, charge trapping and ejection regions were smooth and regular compared with (ALA) films. This means that (A/LAO/A) structure is more stable than the (ALA) structure when exposed to an applied voltage and the associated electric field.

Fig. 3 shows the fully erased, and then programmed and erased *C–V* curves of the (A/LAO/A) films. In the optimum operation conditions of the (A/LAO/A) films, the memory window (ΔV_{th}: V_{th}(program) − V_{th}(erase)) was about 3.13 V. On the other hand, the memory window of the (ALA) films was 1.31 V according to a previous report [12]. Each memory

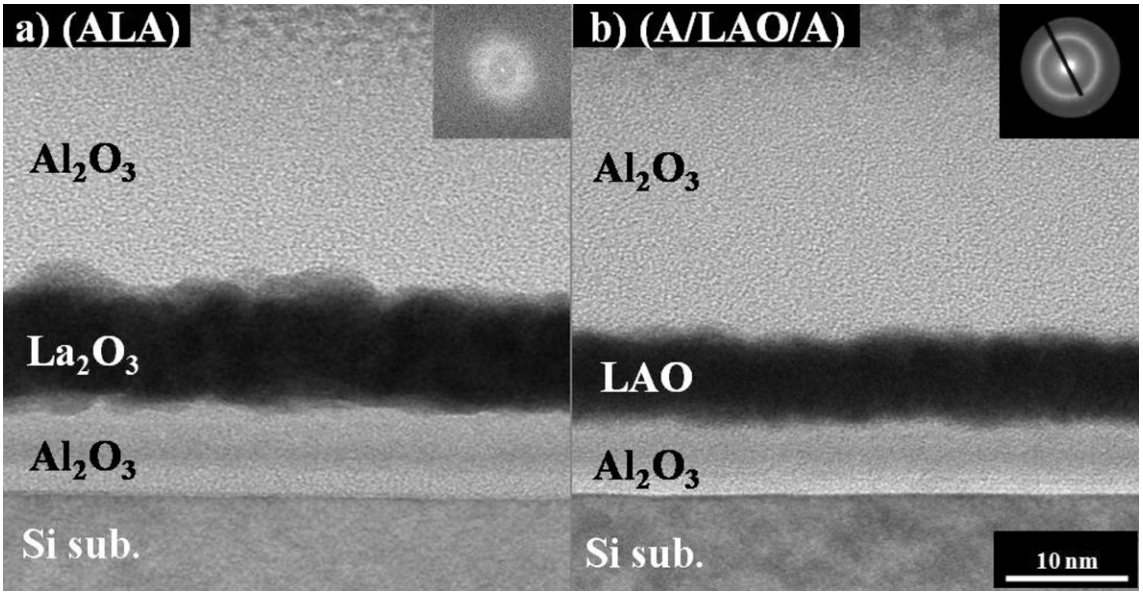

Fig. 1. TEM images of the (a) (ALA) and (b) (A/LAO/A) films.

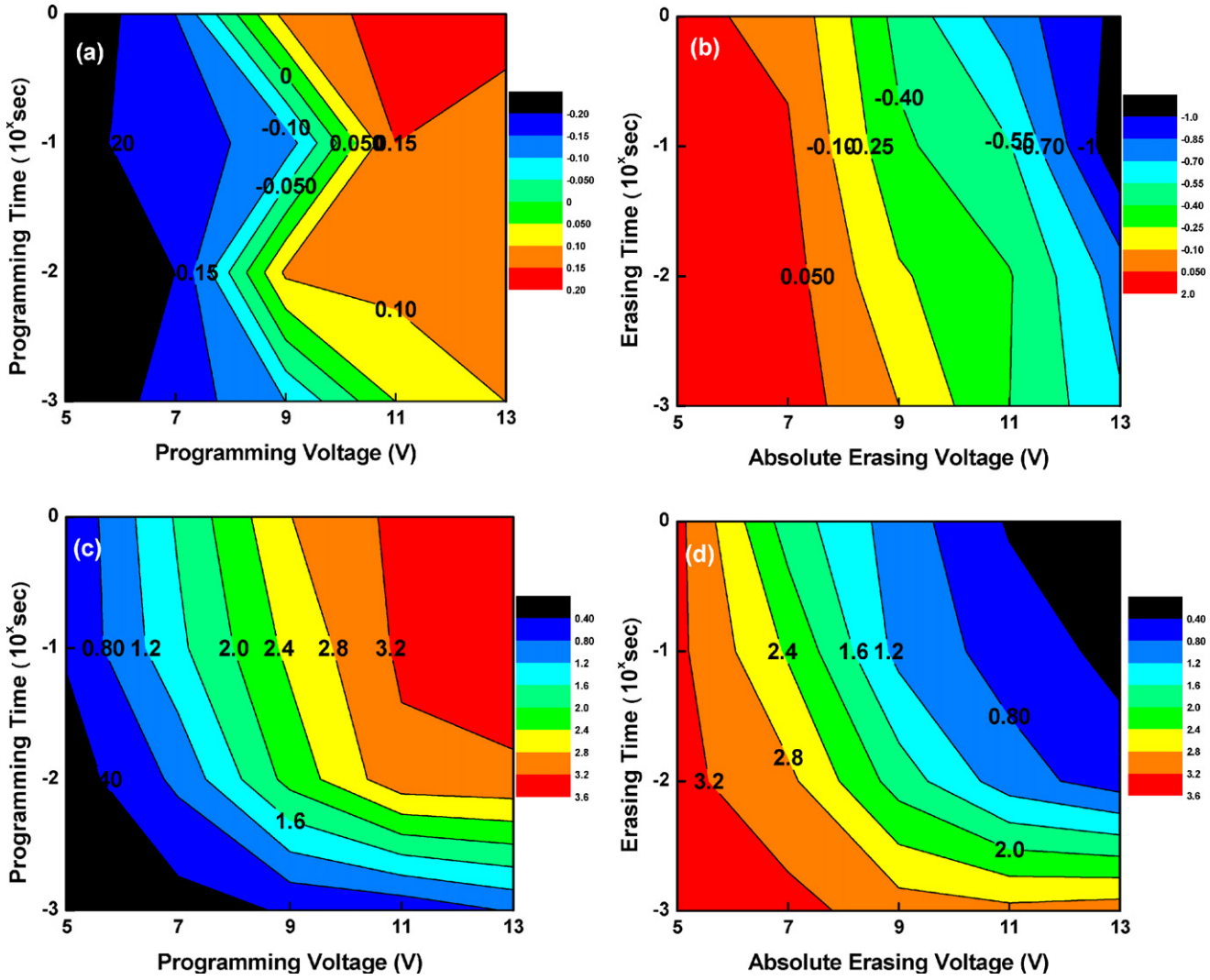

Fig. 2. Threshold voltage (V_{th}) distributions of the (a) program mode and (b) erase mode in the (ALA) films, and (c) program mode and (d) erase mode in the (A/LAO/A) films.

window was measured at the same conditions. According to Ham et al. [13], the difference in memory window gradually decreases to about 40% of the initial memory window after 10 years. Since durability of devices should be guaranteed for about 10 years (over 10^5 program/erase cycles) and the sense amplifier is limited to about 0.6–0.7 V of ΔV_{th}, the initial value of memory window should be at least 3 V. Thus, (A/LAO/A) films are superior to (ALA) films since the initial memory window of 3.13 V in the (A/LAO/A) films would be reduced to 1.252 V after 10 years, still allowing the sense amplifier to sufficiently operate.

In addition, (A/LAO/A) films have an advantage compared with (ALA) films in the defect energy level of the charge. According to Sen et al. [14] and Xiong et al. [15], La_2O_3 has 3 dominant defect types (V_o^0, V_o^+ and V_o^{2+}). The defect energy levels of V_o^0, V_o^+ and V_o^{2+} are below 1.7 eV, 1.4 eV and 1.1 eV from the energy level of the conduction band edge, and $LaAlO_3$ has 4 dominant defect types (V_o^0, V_o^+ and V_o^{2+}) including an additional defect of Al_{La}^O. However, defect energy levels of V_o^0, V_o^+, and V_o^{2+} are below 0.8 eV, 0.6 eV, and 0.55 eV from the energy level of the conduction band edge [14,15]. This

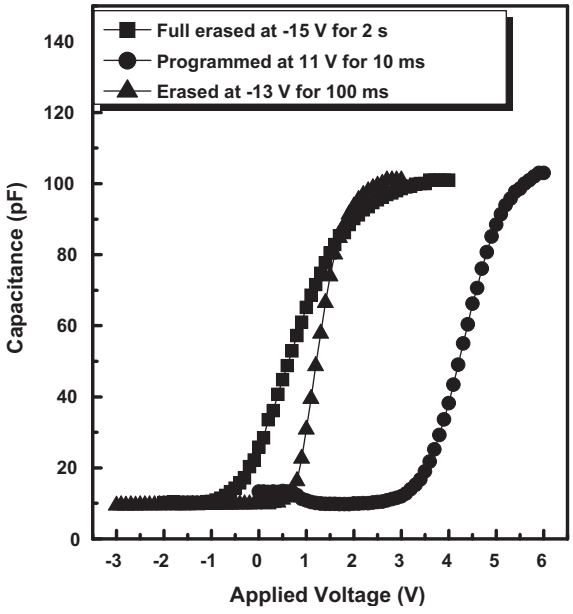

Fig. 3. Fully erased, and then programmed and erased *C–V* curves of the (A/LAO/A) films.

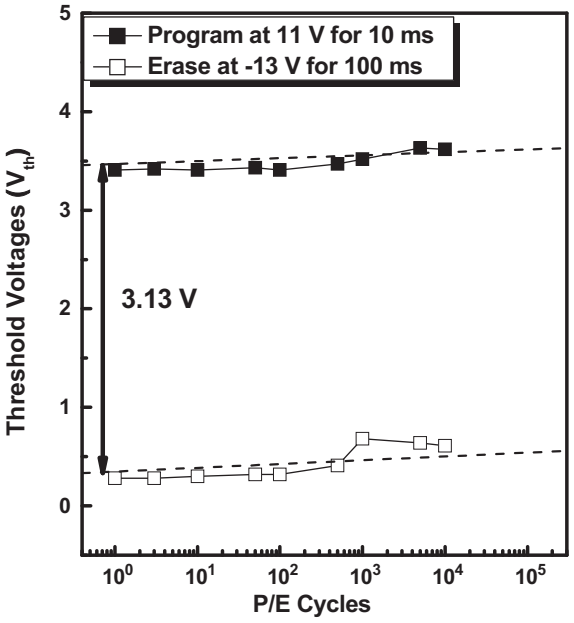

Fig. 4. Threshold voltages (V_{th}) of the (A/LAO/A) films as a function of the number of program/erase cycles in the endurance test.

means that superior charge ejecting phenomenon can occur in the (A/LAO/A) films during erase operation due to the shallow defect energy level. In general, the charge carrier (i.e., electron) is easily ejected at the defect energy state during the erasing operation. In addition, decreasing the voltage and time required for the erase operation has been of recently interest in the flash memory industry. Hence, the efficiency of charge ejection was degraded in the case of deep charge trapping, which means that the charge carrier was trapped at the low defect energy state, resulting in a big difference in energy level of conduction band offsets. Since the height of the electrical barrier is high, the probability of charge ejection decreases, leading to fixation of trapped charges in the (ALA) films.

Fig. 4 shows threshold voltages (V_{th}) of the (A/LAO/A) films as a function of the number of program/erase cycles in the endurance test. In our previous endurance results for (ALA) films, a memory window of 1.3 V was maintained over 10^4 program/erase (P/E) cycles [16]. For (A/LAO/A) films, a memory window of 3.13 V was also maintained over 10^4 P/E cycles. Operation conditions of the P/E cycles for all films were 11 V for 10 ms in the program mode and −13 V for 100 ms in the erase mode. In general, P/E cycles should be maintained until at least 10^5 cycles. Results of linear fitting of our data show that the memory properties could be sufficiently maintained up to about 10^5 cycles. Hence, we conclude that (A/LAO/A) films can be used in flash memory devices instead of conventional ONO (SiO_2–nitride–SiO_2) structures [17].

4. Conclusions

In this paper, we reported charge trap characteristics of Al_2O_3/La_2O_3/Al_2O_3 (ALA) and Al_2O_3/$LaAlO_3$/Al_2O_3 (A/LAO/A) multi-stacked films to replace the conventional ONO structure. An interfacial layer ($Al_xSi_yO_z$) was not observed at a deposition temperature of 350 °C in either film. Memory characteristics of the (A/LAO/A) films were superior to those of the (ALA) films for the same operation conditions. Memory windows of the (A/LAO/A) and (ALA) films were 3.13 V and 1.31 V. Since defect energy levels of the (A/LAO/A) films were higher than those of the (ALA) films, shallow charge trapping was induced, which caused good electrical properties. The (A/LAO/A) films in the P/E cycles test were maintained for up to 10^4 cycles and extrapolation showed no changes up to a minimum of 10^5 cycles. According to these results, (A/LAO/A) films are more suitable than (ALA) films for replacing the conventional ONO structure in flash memory devices.

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